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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
VLAHOS, SOPHIA	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,230	DROGI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28,30,31,34-68,71-76 and 78-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28,30,31,34-68,71-76 and 78-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/10/2005, 12/11/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 1 is objected to because of the following informalities:

Claim 1 (claim set received on 2/13/2006), lines 5-6, recites: "...the single bit **sigma delta** modulator..." However, previously (line 3) only a single bit modulator is mentioned. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 9 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

With respect to claim 9, the claimed: "the low voltage output swing between a high logic level and a low logic level is less than an output swing between a high logic level and a low logic level of a three volt complementary metal oxide semiconductor (CMOS) process technology" is not disclosed in the specification.

With respect to claim 22, the claimed: "wherein the low frequency reference clock synchronizes a sigma delta clock of the radio frequency integrated circuit with a local

clock of the digital signal processing integrated circuit" is not disclosed in the specification.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claims 1, 3, 6-19, 21, 23, 25, 27, 29-31, 34-36, 38, 40-41, 43-44, 46-47, 54-55, 57, 61,71-73, 75-76,78-79, 81, 82-83, 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717).

With respect to claim 1, Maligeorgos et. al., disclose: a radio frequency integrated circuit (RF transceiver of Fig. 2D and Fig. 4 (where more details are shown) see column 10, lines 41-46, column 11, lines 22-25) including a single bit modulator to convert an analog signal into a serial digital bit stream (Fig. 4, ADC circuitry block 418, column 13, lines 36-39, and column 21, lines 48-51 where the ADC is a sigma-delta (modulator) type ADC) and an output driver coupled to the single bit sigma delta modulator, the output driver to drive the serial digital bit stream out from the radio frequency integrated circuit (column 13, lines 42-43, 48-49, also column 15, lines 46-63, column 26, lines 20-25, Fig. 11 data driver 1154 generating differential data signals); and a digital signal processing integrated circuit (Fig. 2D, block 120 baseband

processor, column 9, lines 35-39) including an input receiver coupled to the output driver of the radio frequency integrated circuit (Fig. 2D, block 2121 "Receiver Digital Circuitry" details shown in Fig. 4), the input receiver to receive the serial digital bit stream (see column 16, lines 47-50 where DAC circuitry 445 of Fig. 4 is optional),

Maligeorgos et. al., do not expressly teach: a decimator coupled to the input receiver, the decimator to receive the serial digital bit stream, lower a sampling rate of the serial digital bit stream and convert the serial digital bit stream into parallel digital data samples.

In the same field of endeavor, Behrens et. al., disclose: a decimator coupled to the input receiver (Fig. 17A or 17B and Fig. 23 (details of CIC filter that includes a decimator) see column 39, lines 22-25, where the CIC filter is coupled to the digital differential signals 421 and 424 see column 12, lines 49-53), the decimator to receive the serial digital bit stream (see Fig. 17A and Fig. 23 decimator 2309, column 39, lines 39-40), lower a sampling rate of the serial digital bit stream (column 39, 30-34, decimation by 16 corresponds to lowering of a sampling rate, see also column 41, lines 25-32) and convert the serial digital bit stream into parallel digital data samples (column 40, lines 3-5 where the CIC (that comprises a decimator) functions as an FIR filter – i.e. a moving average FIR) reading onto the claimed limitation "convert the serial digital bit stream into parallel digital data samples" where in the specification of the instant application is explained as: "The serial bit stream to parallel word conversion provided by the decimators 916I,916Q is essentially a digital averaging process of the incoming serial bit stream and not an ordinary serial to parallel

conversion" paragraph [0132])).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al., based on the teachings of Behrens et. al., i.e. to include a decimator coupled to the input receiver, the decimator to receive the serial digital bit stream, lower a sampling rate of the serial digital bit stream and convert the serial digital bit stream into parallel digital data samples, and the motivation behind such a modification is to reduce power consumption (in subsequent stages of the Maligeorgos et. al., system) (see column 41, lines 30-32 of Behrens et. al.).

With respect to claim 3, Maligeorgos et. al., disclose: wherein the single bit modulator is a single bit sigma delta modulator (see column 21, lines 49-51 and column 13, lines 36-39).

With respect to claim 6, Maligeorgos et. al. disclose: wherein the output driver has a low voltage output swing, the output driver to drive the serial digital bit stream out of the radio frequency integrated circuit with the low voltage output swing (see column 23, lines 50-55 see low voltage swing of the differential signal, column 26, lines 23-25).

With respect to claim 7, Maligeorgos et. al. disclose: wherein the input receiver to receive the serial digital bit stream with the low voltage output swing (see Fig. 11, see differential signals (with low voltage swing) on 960 and 965 are received by the receiver digital Circuitry (shown as block 212 in Fig. 2D, column 23, lines 50-55).

With respect to claim 8, Maligeorgos et. al. disclose: wherein the input receiver further to increase the low voltage output swing of the serial digital bit stream within the digital signal processing integrated circuit (see Fig. 11, 1120 receiving differential signal having low-voltage swing see conversion to full-swing signals column 28, lines 50-53 where the function of the replica component 1120A is described).

With respect to claim 9, Maligeorgos et. al. disclose: wherein the low voltage output swing between a high logic level and a low logic level is less than an output swing between a high logic level and a low logic level of a complementary metal oxide semiconductor (CMOS) process technology (see column 30, lines 43-45, conversion to CMOS logic levels, and column 23, lines 50-55, where the logic signals have low voltage swings lower than the supply voltage).

Although neither Maligeorgos et. al. nor Behren et. al., expressly teach: a three volt complementary metal oxide semiconductor, the specific volt level (3 volt) i.e. the supply level of the CMOS depends on the design of the CMOS and it would have been

obvious to a person skilled in the art to use a 3 volt CMOS depending on the specific system requirements and available supply voltage.

With respect to claim 10, neither Maligeorgos et. al. nor Behren et. al expressly teach: wherein the low voltage output swing between a high logic level and a low logic level is less than an output swing between a high logic level of 1.8 volts and a low logic level of 0.2 volts.

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behren et. al., so that low voltage output swing between a high logic level and a low logic level is less than an output swing between a high logic level of 1.8 volts and a low logic level of 0.2 volts, and the motivation to perform such a modification i.e. set specific low voltage swing between a high logic level of 1.8 and a low logic level 0.2, depends on the particular application, available components, and design requirements.

With respect to claim 11, Maligeorgos et. al. disclose: wherein the output driver translates first voltage levels of a first output voltage swing of the serial digital bit stream (see Fig. 11, where signals 1152 supplied to driver 1154 are 1 bit differential voltage signals, column 26, lines 15-21, column 23, lines 49-50 and has a specific voltage swing) into second voltage levels with a second output voltage swing less than the first output voltage swing (see column 26, lines 22-25, differential voltage signals ION and IOP, column 23, lines 50-55) , and the input receiver translates the second voltage

levels of the second output voltage swing into third voltage levels with a third output voltage swing greater than the second output voltage swing (full swing conversion see Fig. 11, 1120 receiving differential signal having low-voltage swing see conversion to full-swing signals column 28, lines 50-53 where the function of the replica component 1120A is described).

With respect to claim 12, Maligeorgos et. al. disclose: wherein the third voltage levels are substantially the same as the first voltage levels (Fig. 11A 1154 reduces the voltage swing whereas full-swing signals are obtained by 1120 (i.e. converted to the first levels that were reduced to the low voltage swing) .

With respect to claim 13, Maligeorgos et. al. disclose: wherein the output driver is double ended and generates a differential signal to represent the serial digital bit stream (Fig. 11A, driver 1154 is double ended i.e. generates differential signal); , and the input receiver has a differential input to receive the differential signal to represent the serial digital bit stream (Fig. 11A receiver digital circuitry side receives 960, 965 differential signals).

With respect to claim 14, Maligeorgos et. al. disclose: wherein the output driver is a low voltage differential signaling transmitter to generate a low voltage differential output signal with a low voltage differential swing (see column 23, lines 45-55 use of differential signals with low swing, and Fig. 11A transmit driver 1154 and receive driver

1122B), and the input receiver is a low voltage differential signaling receiver to receive the low voltage differential output signal with the low voltage differential swing (column 23, lines 45-55).

With respect to claim 15, neither Maligeorgos et. al. nor Behren et. al., disclose: wherein the low voltage differential swing is at least 100 milli-volts. With respect to the specific value of the voltage swing, at the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behren et. al. so that the low voltage differential swing is at least 100 milli-volts depending on the system and component specifications.

With respect to claim 16, Maligeorgos et. al. disclose: wherein the serial digital bit stream is a rectangular waveform (the output of a sigma-delta ADC is theoretically a rectangular output).

With respect to claim 17, Maligeorgos et. al. disclose: wherein the radio frequency integrated circuit is a receiver (see Fig. 4, receiver side (top portion of transceiver of Fig.4) also see Fig.2D block "receiver analog circuitry).

With respect to claim 18, see above rejection of claim 17.

With respect to claim 19, Maligeorgos et. al. disclose: wherein a delta sigma clock is coupled to the single bit sigma delta modulator, a frequency of the delta sigma clock to provide a data rate in the serial digital bit stream (see Fig. 11A, clock signal into ADC 1144, see column 21, lines 48-53, the delta sigma clock, and with respect to the claimed "a frequency of the delta sigma clock to provide a data rate in the serial digital bit stream" see Fig. 11 where the clock signal into the ADC determines the sampling rate of the ADC, i.e. the data rate of the digital signal is determined).

With respect to claim 21, Maligeorgos et. al. disclose: wherein a low frequency reference clock couples between the radio frequency integrated circuit and the digital signal processing integrated circuit to synchronize clock signals of each (see Fig. 35B, where the Reference generator circuitry (TCXO) supplies a common system clock to the RF integrated circuit (of Fig. 2D) and the (DSP /the baseband processor) i.e. the clock signals of each circuitry are synchronized since they are based on a common system clock column 66, lines 10-15 (where the supplied 13MHz is the low reference frequency (compared to the 26MHz frequency), lines 39-43).

With respect to claim 23, Maligeorgos et. al. disclose: at least one gain amplifier to couple to an antenna to receive a first wireless radio frequency signal of a first selectable carrier frequency (see Fig. 8, elements 130, 202, antenna and antenna interface circuitry, element 824 LNA, see column 17, lines 58-65, column 18, lines 54-59, where the "a first selectable carrier frequency" corresponds the frequency

synthesized from the PLL 840 for use at the downconverter); at least one down converter coupled to the at least one gain amplifier (Fig. 8, element 409, downconverter, see column 19, lines 5-14 function of downconverter), the at least one down converter to extract a first analog signal from the first wireless radio frequency signal; at least one single bit sigma delta modulator coupled to the at least one down converter (Fig. 8, ADC circuitry block 836, column 19, lines 20-24, for sigma – delta modulator A/D see column 21, lines 47-51), the at least one single bit sigma delta modulator to convert the first analog signal into a first serial digital bit stream (see Fig. 8. I and Q streams digitized by ADC); and at least one output driver coupled to the at least one single bit sigma delta modulator (not shown in Fig. 8, part of the interface between receiver digital circuitry 851, and receiver analog circuitry 839, shown in Fig. 11, and includes output driver 1154) the at least one output driver to provide a low voltage output swing of the first serial digital bit stream to reduce noise generation as the first serial digital bit stream is coupled to another integrated circuit (see column 23, lines 45-55).

With respect to claim 25,Maligeorgos et. al. disclose: wherein the at least one gain amplifier is a variable gain amplifier or a switched gain amplifier (column 18, lines 55-57).

With respect to claim 27, Maligeorgos et. al. disclose: wherein the radio frequency integrated circuit is a radio frequency receiver integrated circuit (see column 8, lines 47-49, see transceiver chipset).

With respect to claim 29, Maligeorgos et. al. disclose: wherein the first selected carrier frequency is selected from a set of carrier frequencies of a first selected wireless communication system (see column 17, lines 58-65, and column 18, lines 46-57 selection of GSM, DCS, PCS frequency bands and RF PLL circuitry).

With respect to claim 30, Maligeorgos et. al. disclose: the first selected wireless communication system is selected from the set of: Global System for Multiple Communication (GSM) (see Fig. 8, GSM data stream 803).

With respect to claim 31, claim 31 is rejected similarly to claim 30 above.

With respect to claims 34, 35, 40 these claims are rejected based on rationale similar to the one used to reject claim 6 above assuming the claimed first, second, and third signals corresponding to (GSM, DCS, PCS signals as shown in Fig. 8) are processed separately.

With respect to claim 36, Maligeorgos et. al., disclose: wherein the first wireless radio signal and the second wireless radio signal are simultaneously received (Fig. 8, see simultaneous reception of GSM, DCS, PCS RF signals, column 18, lines 46-49).

With respect to claim 38, Maligeorgos et. al., disclose: wherein the first wireless radio signal is received during the time period that the second wireless radio signal is received (see simultanesously received GSM, DCS, signals column 18, lines 46-49).

Claim 41 is rejected based on a rationale similar to the one used to reject claim 36 above.

With respect to claims 43-44, claims 43-44 are rejected similarly to claims 8 and 1 respectively.

With respect to claim 46, Maligeorgos et. al. disclose: wherein the transmitting of the first serial digital data signal is over a single wire (see column 13, lines 48-49,sinle ended signals understood to be transmitted on a single wire).

With respect to claim 47, Maligeorgos et. al. disclose: wherein the first serial digital data signal is a differential data signal, and the transmitting of the first serial digital data signal is over a pair of wires (see column 13, lines 48-49 differential signals understood to be transmitted over pair of wires as shown in Fig. 11).

With respect to claim 54, claim 54 is rejected based on a rationale similar to the one used to reject claim 35 above.

With respect to claim 55, Maligeorgos et. al. disclose: wherein the first serial digital data signal is a complex differential data signal flowing over two pairs of wires (see Fig. 11, differential signals 1146A and 1146B corresponding to differential I and Q signals), an in-phase differential data signal of the first serial digital data signal flows over a first pair of wires, and a quadrature differential data signal with respect to the in-phase differential data signal of the first serial digital data signal flows over a second pair of wires.

With respect to claim 57, Maligeorgos et. al. disclose: a third serial digital data signal flowing from the DSP integrated circuit to the radio frequency integrated circuit, the third serial digital data signal representing a first transmit data signal for communication over the first wireless communication system (see Fig. 8, transmit side, signals I and Q 460 and 463, to be transmitted in GSM or DCS/PCS).

With respect to claim 58, Maligeorgos et. al. disclose: wherein the third serial digital data signal is a complex differential data signal flowing over two pairs of wires, an in-phase differential data signal of the third serial digital data signal flows over a first pair of wires, and a quadrature differential data signal with respect to the in-phase differential data signal of the third serial digital data signal flows over a second pair of

wires (see Fig. 8, where lines 460 and 463 correspond to the two pairs of wire carry differential I and Q signals).

With respect to claims 60-61, claim 60 is rejected based on rationale similar to the one used to reject claim 6 above and 61 on rationale similar to the one used to reject claim 53 above.

With respect to claims 71-72, 73 claims 71 -72 are rejected similarly to claim 6 above and claim 73 is rejected similarly to claim 7 above.

With respect to claims 75-76 claims 75-76 are rejected similarly to claims 23 and 27 respectively.

With respect to claims 78-79, claims 78-79 are rejected similarly to claims 1 above.

With respect to claims 82-83, claims 82-83 are rejected similarly to claims 1 above.

6. Claims 2,45, 74, 80-81, 8-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717) and Kim et. al., (U.S.7,035,595).

With respect to claim 2, neither Maligeorgos et. al nor Behrens et. al expressly teach: wherein the digital signal processing integrated circuit further includes a demodulator to digitally demodulate the parallel digital data samples into data words for further signal processing by the digital signal processing integrated circuit.

In the same field of endeavor, Kim et. al., disclose: wherein the digital signal processing integrated circuit further includes a demodulator to digitally demodulate the digital data samples into data words for further signal processing by the digital signal processing integrated circuit (see Fig. 2A, DSP 212, column 4,lines 50-56).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al and Behrens et. al based on the teachings of Kim et. al., so that the digital signal processing integrated circuit further includes a demodulator to digitally demodulate the parallel digital data samples (i.e. the averaged digital samples of claim 1) into data words for further signal processing by the digital signal processing integrated circuit, and the motivation to perform such a modification is that DSPs are used for signal processing (and are reconfigurable and programmable depending on the specific application) and such signal processing includes demodulation (also equalization, filtering)(Kim et. al., column 4, lines 39-42).

With respect to claim 45, claim 45 is rejected based on a rationale similar to the one used to reject claim 2 above.

With respect to claims 80-81, and 84-85 these claims are rejected based on a rationale similar to the one used to reject claim 2 above. (With respect to the claimed "the processor includes programmable instructions" of claims 81 and 85 see column 11, lines 22-31 of Maligeorgors et. al (software and/or hardware combination)).

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717) and Sangil Park, "Principles of Sigma-Delta for Analog-to-Digital Converters", APR8 /Rev. 1, (1993)).

With respect to claim 4, neither Maligeorgos et. al. nor Behrens et. al., expressly teach: wherein the single bit modulator is a single bit delta modulator. In the same field of endeavor (A/D conversion using modulators) Park discloses: a single bit delta modulator (section 5 "Delta Modulation" see Fig. 5-1).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behrens et. al.,
based on the teachings of Park, so that the single bit modulator is a single bit sigma delta modulator, since in theory the spectrum of quantization noise of the prediction error (output of the delta modulator) is flat and the noise level is set by the 1 bit comparator (see last paragraph on page 5-1 of Park).

With respect to claim 5,neither Maligeorgos et. al. nor Behrens et. al., expressly teach: wherein the single bit modulator is a single bit analog to digital converter and a modulator coupled together.

In the same field of endeavor, (A/D conversion using modulators) Park discloses: the single bit modulator is a single bit analog to digital converter and a modulator coupled together (Fig.6-4, see 1 bit output, 1-bit quantizer (A/D converter) and the modulator is the dotted box , and description starting on the second paragraph of page 6-4)

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behrens et. al., based on the teachings of Park, so that the single bit modulator is a single bit analog to digital converter and a modulator coupled together (as in the A/D converter shown in Fig. 6-4) since the performance does not depend on the frequency (rate of change) of the signal and when filtered the output result is very precise (first paragraph on page 6-5))/

Claims 48-50, 56, 58-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717) and Prentice (U.S. 6,674,988).

With respect to claim 48, Malegoergos et. al., disclose: wherein the first serial digital data signal is a complex differential data signal and the transmitting of the first

serial digital data signal is over two pairs of wires (Fig. 11, signals to be transmitted up to multiplexer 1150 in block 910, see I and Q differential signals),

Maligeorgos et. al., do not teach: a first differential data signal of the first serial digital data signal is transmitted over the first pair of wires, and a second differential data signal of the first serial digital data signal is transmitted over the second pair of wires.

In the same field of endeavor, Prentice discloses: a first differential data signal of a data signal is transmitted over the first pair of wires, and a second differential data signal of a digital data signal is transmitted over the second pair of wires (Fig. 2, see drivers 232 and 234 for I and Q differential signal transmission).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgoe et. al.,based on the teachings of Prentice , i.e. so that a first differential data signal of the first serial digital data signal is transmitted over the first pair of wires, and a second differential data signal of the first serial digital data signal is transmitted over the second pair of wires, and the motivation to perform such a modification, would be obvious to a person skilled in the art depending on the number of available components (drivers), space, and power consumption constraints.

With respect to claims 49 and 50 the limitations of these claims are rejected above in claim 48 (where the real and imaginary components are interpreted to correspond to in-phase and quadrature signal components of the data).

With respect to claims 58-59, these claims are rejected based on a rationale similar to the one used to reject claims 49-50 above.

7. Claims 51, 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717) , Prentice (U.S. 6,674,988) and Fitzpatrick et. al., (U.S. 6,266,517).

With respect to claim 51, claim 51 is rejected based on a rationale similar to the one used to reject claim 48 above, and with respect to the limitations not expressly disclosed by Maligeorgos et. al., Behrens et. al. or Prentice: a magnitude data signal and a phase data signal, these limitations are disclosed by Fitzpatrick et. al (see Fig. 2, Cartesian to polar conversion block 242,) and the Fitzpatrick et. al (not in the field of transceivers) reference is used as evidence of representing I/Q in terms of magnitude and phase (see Fig.9 of Fitzpatrick et. al.).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al., ,Behrens et. al., (U.S. 6,970,717) , and Prentice (U.S. 6,674,988) based on the teachings of Fitzpatrick et. al (relating to complex signal representation I/Q conversion to polar coordinates) and the motivation to perform such a modification, (to represent the I/Q signal of Maligeorgos as a magnitude/phase) relates to choosing a specific signal representation (I/Q which can be expressed as magnitude and phase) and therefore would have been obvious to a person skilled in the art at the time of the invention.

With respect to claims 56, claim 56 is rejected based on a rationale similar to the one used to reject claim 51.

8. Claims 20, 22, 24, 26, 37, 42, 62-64, 66-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717) and Khlat et. al. (U.S. 2004/0038652).

With respect to claim 20, neither Maligeorgos et. al. nor Behrens et. al expressly teach: wherein the frequency of the delta sigma clock is programmable to provide various data rates in the serial digital bit stream for various wireless communication systems.

In the same field of endeavor, Khlat et. al., disclose: wherein the frequency of the delta sigma clock is programmable to provide various data rates in the serial digital bit stream for various wireless communication systems (see Fig. 2, where the sigma-delta modulators have fs sampling frequencies, and block 199 generates the sampling frequencies for the different system modes (paragraph [0013] and see table 1 different sampling frequencies and paragraph [0022] where PLL generates the frequencies (clocks for the ADC)).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behrens based on the teachings of Khlat et. al., so that the frequency of the delta sigma clock is programmable to provide various data rates in the serial digital bit stream for various wireless communication

systems and the motivation to perform such a modification is reception of signals of different standards (for example GSM clock frequency is 13MHz, see Maligeorgos et. al. column 11, lines 50-52 and Khlat et. al., Table 1, (sampling frequency) whereas other standards require different sampling clocks see table 1 of Khlat et. al.)).

With respect to claim 22, neither Maligeorgos et. al. nor Behrens disclose: wherein the low frequency reference clock synchronizes a sigma delta clock of the radio frequency integrated circuit with a local clock of the digital signal processing integrated circuit.

In the same field of endeavor, Khlat et. al., disclose: synchronizing a sigma delta clock of the radio frequency integrated circuit with a clock (see fig. 5, fractional PLL generating sigma delta clocks).

At the time of the invention, it would have been obvious to modify the system of Maligeorgos et. al. and Behrens based on the teachings of Khlat et. al., so that the low frequency reference clock synchronizes a sigma delta clock of the radio frequency integrated circuit with a local clock of the digital signal processing integrated circuit and the motivation to perform such a modification is to generate stable sigma-delta clock(s) using PLL based frequency synthesis

With respect to claim 24, Maligeorgos et. al. disclose: further comprising a second gain amplifier to couple to the antenna to simultaneously receive a third wireless

radio frequency signal of a third selectable carrier frequency (see Fig. 40, second LNA coupled to the receiving antenna, receiving a third wireless signal (the term "third" is arbitrary/relative (?)). The difference between Maligeorgos et. al. and Behrens is that, Maligeorgos et. al. and Behrens do not expressly teach: a second down converter coupled to the second gain amplifier, the second down converter to extract a third analog signal from the third wireless radio frequency signal; a second single bit sigma delta modulator coupled to the second down converter, the second single bit sigma delta modulator to convert the third analog signal into a third serial digital bit stream; and a second output driver coupled to the second single bit sigma delta modulator, the second output driver to provide a low voltage output swing of the third serial digital bit stream to reduce noise generation as the third serial digital bit stream is coupled to another integrated circuit, (i.e. separate processing components for the different wireless standard signals received –that correspond to those claimed in claim 23 to process the first wireless signal).

In the same field of endeavor, (multi-band receivers), Khlat et. al., disclose: a second down converter coupled to the second gain amplifier, the second down converter to extract a third analog signal from the third wireless radio frequency signal (Fig. 5, receiver, bottom processing path, see second amplifier (triangle shown in the RF channel 2 path) I/Q down converter at flo2), ; a second single bit sigma delta modulator coupled to the second down converter, the second single bit sigma delta modulator to convert the third analog signal into a third serial digital bit stream (see at least one of the sigma-delta converters (used to digitize the I and Q components)).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behren et. al., based on the teachings of Khlat et. al., (see separate processing of signals as shown in Fig. 5) so that a second down converter coupled to the second gain amplifier, the second down converter to extract a third analog signal from the third wireless radio frequency signal; a second single bit sigma delta modulator coupled to the second down converter, the second single bit sigma delta modulator to convert the third analog signal into a third serial digital bit stream, is used and the motivation to perform such a modification is to increase the speed of the received signal processing (simultaneous / parallel processing). With respect to the claimed limitation: and a second output driver coupled to the second single bit sigma delta modulator, the second output driver to provide a low voltage output swing of the third serial digital bit stream to reduce noise generation as the third serial digital bit stream is coupled to another integrated circuit, Maligeorgos et. al., disclose: an output driver coupled to the second single bit sigma delta modulator, the second output driver to provide a low voltage output swing of the third serial digital bit stream to reduce noise generation as the third serial digital bit stream is coupled to another integrated circuit, and therefore at the time of the invention,it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behren et. al., so that it includes the second output driver to provide a low voltage output swing of the third serial digital bit stream to reduce noise generation as the third serial digital bit stream is coupled to another integrated circuit, so that interference is

reduced among circuit partitions (see column 15, lines 44-49, column 23, lines 45-55 of Maligeorgos et. al.,)

With respect to claim 26, Maligeorgos et. al., disclose: wherein the at least one gain amplifier and the second gain amplifier are variable gain amplifiers or switched gain amplifiers (column 18,lines 55-57 for embodiment of Fig. 8).

With respect to claim 34, claim 34 is rejected based on a rationale similar to the one used to reject claim 23 above.

With respect to claim 37, neither Maligeorgos et. al. nor Behrens ,disclose: wherein the first analog signal and the second analog signal are simultaneously extracted. However in the same field of endeavor, Khlat et. al., disclose: a first analog signal and a second analog signal are simultaneously extracted (see Fig. 5, parallel processing of analog signals from RF channel 1, RF channel 2, at respective demodulators).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behrens based on the teachings of Khlat et. al., so that wherein the first analog signal and the second analog signal are simultaneously extracted, so that they be processed

With respect to claims 39 and 42, claims 39 and 42 are rejected based on a rationale similar to the one used to reject claim 37 above.

With respect to claim 66, claim 66 is rejected based on a rationale similar to the one used to reject claim above.

With respect to claims 67 and 68, these claims are rejected based on a rationale similar to the one used to reject claims 6 and 25 above.

9. Claims 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Behrens et. al., (U.S. 6,970,717) and Sugar et. al., (U.S. 7,020,451).

With respect to claim 52, Maligeorgos et. al. disclose: up-converting the fourth analog signal to a selectable carrier frequency (see Fig. 4, signals 460 and 463 are considered to correspond to the fourth signal (complex signal) see element 465 baseband upconverter, see also Fig. 8 embodiment); and transmitting the fourth analog signal through the antenna as a fourth wireless radio frequency signal (see Fig. 4, transmit path circuitry).

Neither Maligeorgos et. al., nor Behrens et. al., expressly teach: receiving a fourth serial digital data signal from the DSP integrated circuit for transmission over a wireless communication system; converting the fourth serial digital data signal from the

DSP integrated circuit into a fourth analog signal, i.e. Maligeorgos et. al., and Behrens et. al., do not expressly teach digital to analog conversion of the fourth signal.

In the same field of endeavor, Sugar et. al., disclose: receiving a serial digital data signal from the DSP integrated circuit for transmission over a wireless communication system; converting the serial digital data signal from the DSP integrated circuit into an analog signal (see Fig. 1, DAC conversion of the signal out of the baseband processor (DSP, see column 2,lines 32-37)).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al., and Behrens et. al (that do not show details regarding the baseband processor only analog signals 460, 463 in the transmit path) based on the teachings of Sugar et. al., so that a fourth serial digital signal (generated from the baseband processor) is converted into the fourth analog signal that is processed by block 466 of Fig. 4. The motivation to perform such a modification, would have been obvious to a person skilled in the art, since the baseband circuitry (is a dsp) processes digital signals that have to be converted to analog so that they are transmitted, (and this is well known in the art).

With respect to claim 53, neither Maligeorgos nor Behrens et. al., and Sugar et. al., expressly teach:

wherein the fourth serial digital data signal from the DSP integrated circuit is a low voltage output swing signal and the method further includes increasing the low

voltage output swing in the fourth serial digital data signal from the DSP integrated circuit.

However, Maligeorgos teaches using low voltage output swing digital signals and increasing the low voltage output swing in the serial digital data signal (see Fig. 11A, driver configuration for transferring data signals 960, 965, column 23, lines 45-55 and conversion of the low-voltage swing into full-swing , column 28, lines 50-53 where the function of the replica component 1120A is described).

Therefore based on the teachings of Maligeorgos (applicable to the receive path data transfer), it would have been obvious to a person skilled in the art to modify the system of Maligeorgos nor Behrens et. al., and Sugar et. so that the fourth serial digital data signal from the DSP integrated circuit is a low voltage output swing signal and the method further includes increasing the low voltage output swing in the fourth serial digital data signal from the DSP integrated circuit, and the motivation to perform such a modification is to use differential signals so that interference is reduced (see column 15, lines 45-49, column 23, lines 45-55) with low voltage swing, ie. the fourth serial digital signal to be a low voltage swing signal, and with respect to the limitation: increasing the low voltage output swing in the fourth serial digital data signal from the DSP integrated circuit, using the driver configuration (shown in Fig. 11A where full-swing differential signals are converted to low-voltage swing ones and back to full-swing, so that interference is reduced) taught by Maligeorgos, the fourth serial digital data signal can be transferred in the baseband processor with reduced interference to other transceiver circuits).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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SV
6/8/2007

M. G

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER